CALIBRATION METHODS AND CIRCUITS FOR
OPTIMIZED ON-DIE TERMINATION

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BACKGROUND

[0001]   High-speed data communication integrated circuit (IC) dies are known to include both drivers and receivers. The driver of one such IC connects to the receiver of another via one or more signal transmission lines. Both the driver and receiver circuits include termination elements that attempt to match the characteristic impedance of the transmission line to the output impedance of the driver and input impedance of the receiver, as impedance mismatches degrade signal quality and consequently reduce communication speed and reliability.

[0002]   Some conventional communication systems employ control systems that calibrate the impedance of on-chip termination elements for improved impedance matching. For a detailed discussion of one such system, see U.S. Patent No. 6,418,500 entitled "Feedback Control for Termination Adjustment," which issued on July 9, 2002, to Gai et al.

[0003]   Some high-performance communication systems employ current-mode switching for improved speed performance. Such systems include current-mode drivers, which convey digital signals by modulating current between values representative of different logic levels. The levels of current used to express logic levels are carefully calibrated and controlled to obtain rapid switching and low power consumption. The following issued patents describe conventional circuits for calibrating the drive current for current-mode drivers: U.S. Patent No. 5,254,883 entitled "Electrical Current Source Circuitry for a Bus," which issued on October 19, 1993, to Horowitz et al.,

and U.S. Patent No. 6,462,591 entitled "Semiconductor Memory Device Having a Controlled Output Driver Characteristic," which issued on October 8, 2002, to Garrett et al.

[0004]   The aforementioned calibration techniques for setting and maintaining appropriate termination resistances and drive currents work well in many applications. High-speed circuits are in a very competitive market, however, and must achieve ever greater performance levels to satisfy customer demand. There is therefore a need for area- and power-efficient communication circuits that exhibit improved speed performance.

SUMMARY

[0005]   The present invention is directed to efficient on-die termination (ODT) systems and methods that facilitate high-speed communication between a driver die and a receiver die interconnected via one or more signal transmission lines. An ODT control system in accordance with one embodiment calibrates and maintains the termination resistances and drive currents of the driver die to produce optimal output swing voltages on the signal transmission lines. A similar ODT control system calibrates and maintains the termination resistances of the receiver die. The ODT control systems rely upon external voltage and resistance references for termination resistance and drive current calibration.

[0006]   An ODT control system in accordance with one embodiment calibrates drive current by matching the drive current to a reference current drawn through a precision resistor, and calibrates termination resistance by matching on-die termination elements with the same external resistor. Comparison circuitry employed to match the reference and drive currents is also used to match the reference and ODT resistances. This sharing of resources saves power and die

area. In addition, offset errors introduced by shared
components impact the resistance and current calibrations in
opposite ways, and thus tend to cancel one another.

[0007]   Termination elements in some embodiments are divided
into two adjustable resistive portions, both of which are
designed to minimize capacitive loading. One portion is
optimized to produce a relatively high range of adjustment,
while the other is optimized for fine-tuning and glitch-free
switching. Active ODT control systems can calibrate the first
portion before respective drive and receive circuitry begin
communicating, and can then employ the second portion to
account for resistive drive that occurs due to supply-voltage
and temperature fluctuations. In one embodiment, the second
portion employs a serial, thermometer-coded voltage divider to
provide glitch-free switching between ODT resistance levels.
In another embodiment, the second portion employs an analog
voltage divider. Either embodiment can be used to
periodically calibrate ODT resistance without introducing
undesirable resistive glitches.

[0008]   This summary does not limit the invention, which is
instead defined by the allowed claims.

BRIEF DESCRIPTION OF THE FIGURES

[0009]   Figure 1 is a block diagram of a data communication
system 100 in accordance with one embodiment.

[0010]   Figure 2 depicts a termination resistance and drive
current calibration system 200 that includes ODT control
system 130, reference resistor 175, and reference source 170
of Figure 1.

[0011]   Figure 3 depicts a process 300 employed by control
system 130, as detailed in Figure 2, to calibrate reference
ODT resistor 230 and ODT current Iodt.

[0012]   Figure 4 depicts a communication system 400 in

accordance with another embodiment.

[0013]   Figure 5 details an embodiment of calibration system
200 of Figure 2.

[0014]   Figure 6 depicts an ODT termination element 600 in
accordance with one embodiment.

[0015]   Figure 7 depicts a termination element 700 in
accordance with another embodiment.

DETAILED DESCRIPTION

[0016]   Figure 1 is a block diagram of a data communication
system 100 in accordance with one embodiment. Communication
system 100 includes a first integrated circuit (IC) die 105
connected to a second IC die 110 via a number of signal
transmission lines 115. Die 105 includes a plurality of
identical driver circuits 120 and an on-die-termination (ODT)
control system 130. Control system 130 establishes and
maintains the termination resistances and drive currents of
driver circuits 120 to produce optimal output swing voltages.

[0017]   Die 110 includes a plurality of identical receiver
circuits 125, each of which receives signals from a
corresponding one of driver circuits 120 of die 105. Die 110
includes an ODT control system 187 that establishes and
maintains the termination resistance applied to incoming
signals to optimize the swing voltages of those signals.

[0018]   Each of dies 105 and 110 may be any of myriad types
of processing chips capable of communicating electrical
signals. Typical examples include IC dies that communicate via
parallel or serial bus interfaces. Transmission lines 115 may
be, for example, a wire, a cable, a trace on a printed-circuit
board, a chip etching, a waveguide, or other medium that
allows for transmission of signals.

[0019]   For simplicity, die 105 and die 110 are presumed to
support respective driver and receive circuitry; in other

embodiments, however, die 105 additionally supports receive circuitry, and die 110 additionally supports transmit circuitry. Such embodiments can use either unidirectional or bidirectional signal lines, as is well known to those of skill in the art. Also important, the depicted embodiment is described in connection with a typical case in which two dies communicate signals via external lines, but other embodiments optimize signal line termination resistance, drive current, and signal swing to improve communication speed between circuits that exist on the same die. Driver circuits 120 are identical, as are receiver circuits 125. The following description is limited to the topmost driver/receiver pair for brevity.

[0020]   Driver circuit 120 includes an driver 135 receiving an input data stream represented as a pair of complimentary input signals Din0 and Din0b, which are provided on complimentary driver input nodes having the same designations. (As with other designations herein, Din0 and Din0b refer both to signals and their corresponding nodes; whether a given designation refers to a signal or a node will be clear from the context.) Driver 135 additionally includes a pair of driver output terminals 150 and 155 that connect to signal transmission lines 115 via IC pads (not shown). Driver output terminals 150 and 155 convey complimentary output signals derived from the input data stream. (Unless otherwise defined, terminals, lines, conductors, and traces that carry a given signal fall under the umbrella term "node"; in general, the choice of a given description of a circuit node is a matter of style, and is not limiting.)

[0021]   Driver circuit 120 includes a pair of termination elements 145 and a digital-to-analog converter (DAC) 140. Each of driver output terminals 150 and 155 connects to a reference voltage Vio via a respective adjustable termination element

145, and each termination element 145 receives digital ODT
calibration signals from ODT control system 130 via an ODT
calibration port 165. Driver circuit 120 additionally includes
a current control port 160, which receives digital current-
calibration signals from control system 130. DAC 140 converts
these digital signals into a current-control voltage that
controls the level of drive current provided by driver 135. By
controlling both the termination resistance and the drive
current of driver circuit 120, ODT control system 130
optimizes the swing voltages on driver output terminals 150
and 155, and consequently reduces noise and improves speed
performance.

[0022]   The resistance values of termination elements 145
and the drive current provided by driver 135 vary with
process, voltage, and temperature. ODT control system 130
therefore relies upon precise reference components to
establish appropriate termination resistances and drive
currents. In the depicted embodiment, die 105 is connected to
a first reference voltage Vr1 through an external voltage
source 170 and an external precision resistor 175. Reference
source 170 conveys a second reference voltage Vr2 to ODT
control system 130. The difference between reference voltage
Vr1 and Vr2 is used to establish an appropriate swing voltage.
Reference resistor 175 conveys a reference-resistor voltage
Vrr to ODT control system 130, acting as a reference
resistance against which to compare and adjust termination
elements 145. A calibration process for establishing the
appropriate resistance through termination elements 145 and
drive currents provided by drivers 135 is described below in
connection with Figures 2 and 3.

[0023]   Receiver circuit 125 within die 110 includes a
differential amplifier 185 connected to a pair of
complimentary signal transmission lines 115 via respective

receiver input terminals 186 and 189. Each of input terminals
186 and 189 connect to reference voltage Vio via a respective
termination element 180. Termination elements 180 are similar
to elements 145 in this embodiment, and are controlled via a
line ODT from an ODT control system 187 similar to system 130.
Control system 187 compares the values of termination elements
180 with an off-chip, precision reference resistor 195 to
account for process, voltage, and temperature variations that
affect the resistance values of termination elements 180. ODT
control system 187 is also capable of calibrating drive
current, though no drivers are shown in Figure 1. Where drive-
current calibration is desired, control system 187 connects to
an external reference voltage 190. Receiver circuit 125
receives the incoming data stream on complimentary input nodes
186 and 189 and presents a resulting data to the interior of
IC die 110 via corresponding data output node Dout0.

[0024]   Figure 2 depicts a termination resistance and drive
current calibration system 200 that includes ODT control
system 130, reference resistor 175, and reference source 170
of Figure 1. (In general, the first digit of a given numerical
designation indicates the Figure in which the indicated
element was introduced. For example, reference resistor 175
was introduced in Figure 1.)

[0025]   Reference source 170 and reference resistor 175 are
external, precision elements connected to system 130 via a
pair of pads 201 and 202. Control system 130 includes a
comparator 215, an analog multiplexer 220, a reference ODT
resistor 230, and a current source 240. Control system 130
calibrates the resistance value Rodt of resistor 230 to match
the reference resistance Rref of external precision resistor
175. Control system 130 also matches the current Iodt through
resistor 230 with a reference current Irr through reference
resistor 175 to produce a desired voltage drop across ODT

resistor 230. ODT counter 245 stores a digital value
representative of the offset required to calibrate IDT
resistor 230, and a current-control counter 250 stores a
digital value representative of the offset required to
calibrate current source 240. The digital values from counters
245 and 250 are then conveyed throughout die 105 (Figure 1) to
calibrate similar or identical termination elements and
current sources within driver circuits 120.

[0026]   Figure 3 depicts a process 300 employed by control
system 130, as detailed in Figure 2, to calibrate reference
ODT resistor 230 and ODT current Iodt. First, at step 305,
current-calibration signal ICAL1b, an active-low signal, is
asserted. Analog multiplexer 220 thus selects second reference
voltage Vr2 for comparison with reference voltage Vrr from
resistor 175. The inverse of signal ICAL1b, ICAL1, enables
current-control counter 250 to increment and decrement in
response to output signals from comparator 215.

[0027]   Current source 240 pulls reference current Irr
through reference resistor 175. Per Ohm's law, reference
voltage Vrr equals reference voltage Vr2 when the product of
reference current Irr and reference resistance Rref equals the
swing voltage Vsc across voltage reference 170 (i.e., when
Irr*Rref= Vsc). Comparator 215 compares voltage Vrr with
voltage Vr2 (decision 310), and adjusts the contents of
current-control counter 250 as necessary to render voltage Vrr
equivalent to voltage Vr2 (step 315). For example, if
comparator 215 determines that Vrr is lower than Vr2,
comparator 215 increments counter 250 to reduce current Irr,
and consequently increase the voltage Vrr. The comparison and
adjustment of steps 305, 310, and 315 continue until Vrr and
Vr2 are substantially equal. At this point, current counter
250 stores a count CCNT that offsets the current Irr provided
by current source 240. ODT current Iodt is substantially equal

to reference current Irr, so steps 305, 310, and 315 place current Iodt at or near the expected operating level.

[0028]   The granularity of current-control count CCNT introduces some uncertainty as to the exact reference current Irr and corresponding Iodt. Employing more register bits and associated bus lines for CCNT reduces this uncertainty at a cost of increased overhead.

[0029]   The next portion of calibration process 300 sets resistance Rodt of resistor 230 substantially equal to reference resistance Rref of precision resistor 175 (i.e., Rodt≈Rref) by adjusting the count in counter 245. The first current-calibration signal ICAL1b is deasserted (held to a logic one), causing multiplexer 220 to apply voltage Vodt from resistor 230 to the second input terminal of comparator 215. Deasserting ICALb also disables counter 250, freezing current control signal CCNT to hold Iodt and Irr constant. A termination calibration signal TCAL to counter 245 is asserted, enabling counter 245 to increment and decrement in response to output signals from comparator 215.

[0030]   In step 320, comparator 215 compares Vrr and Vodt. ODT counter 245 increments or decrements in response to the output of comparator 215, altering the resistance Rodt through ODT element 230. The input voltage Vio to termination resistor 230 is connected to off-chip voltage reference Vr1, and is therefore substantially equivalent to voltage Vr1. Because the currents Irr and Iodt are substantially identical, Ohm's law provides that voltage Vodt is substantially equal to voltage Vrr if resistance Rodt of resistor 230 matches reference resistance Rref of precision resistor 175. Comparator 215 thus adjusts the contents of counter 245 (step 330) until decision 325 determines that voltages Vrr and Vodt are substantially equal. The granularity of ODT-control count ODT introduces some uncertainty as to the exact reference resistance Rodt.

This uncertainty can be improved by employing more register bits within counter 245, but this improvement comes at a cost of increased overhead.

[0031]   Input/output voltage Vio, being distributed on chip, may vary by some small amount from external reference voltage Vrl. The resulting uncertainty combines with other uncertainties, such as those resulting from the measurement granularities of counters 245 and 250, to produce still greater uncertainty. A second current-calibration sequence recalibrates ODT current Iodt using the calibrated ODT resistor 230 and input voltage Vio to reduce this uncertainty.

[0032]   Returning to Figure 1, each signal transmission line 115 includes an associated pair of termination elements 145 and 180 connected in parallel between Vio and respective ends of the signal transmission line. To duplicate this arrangement, current control system 130 includes a transistor 255 that shorts reference resistor 175 and ODT resistor 230 in response to a second current-calibration signal ICAL2, effectively connecting resistors 175 and 230 in parallel between node Vio (recall Vrl is an off-chip version of Vio) and node Vodt. Because voltages Vrl and Vio and resistances Rref and Rodt are substantially equal, the expected current between interconnected nodes Irr and Iodt is expected to be quite low.

[0033]   In step 335, signal TCAL is deasserted and both current-control signals ICAL1b and ICAL2 are asserted. Counter 245, and thus resistance Rodt, is thus held constant as comparator 215 once again compares Vrl with Vrr (step 340). Counter 250 increments or decrements in response to output signals from comparator 215 (step 350). The calibration process 300 is complete when system 130 voltages Vr2 and Vrr are substantially equal (step 345). The resulting offsets held in counters 245 and 250 are distributed on buses ODT and CCNT

to drivers and receivers on the same die to establish
appropriate ODT resistances and drive currents in the manner
described above in connection with Figure 1.

[0034]   The current and resistance calibration steps are
carried out using shared resources, including the low-offset,
high-gain comparator 215. This sharing of resources saves
power and die area. In addition, offset errors introduced by
shared components impact the resistance and current
calibrations in opposite ways, and so tend to cancel one
another. For example, a comparator error that results in a
slightly high ODT resistance Rodt produces a slightly low ODT
current Iodt. Rodt and Iodt are multiplied to produce the
desired swing voltage, so the increase in Rodt tends to cancel
the decrease in Iodt.

[0035]   Figure 4 depicts a communication system 400 in
accordance with another embodiment. System 400 includes
components in common with communication circuit 100 of Figure
1, like-elements being the same or similar. System 400
includes first and second bus interfaces 405 and 410, each of
which is typically a portion of a respective IC die,
interconnected via parallel bus 417. One driver circuit 415 of
interface 405 and a corresponding receive circuit 420 of
interface 410 are detailed: the remaining driver circuits 415
and receive circuits 420 are represented as simple boxes for
brevity.

[0036]   Driver circuit 415 includes a pair of termination
elements 425 (ODT resistors) connected between reference
voltage Vio and respective ones of a pair of signal
transmission lines. Driver 415 additionally includes a
current-controlled amplifier 418, which in turn includes a
pair of input transistors 430 and a current-source transistor
435. Each of transistors 430 connects between one of
termination elements 425 and a power-supply terminal GND via

transistor 435. A DAC 440 within driver circuit 415 controls
the current through transistor 435 by applying a control
voltage CV to the gate of transistor 435, and consequently
controls the maximum voltage drop across termination elements
425.

[0037]   ODT control system 130 derives offsets ODT and CCNT
to calibrate termination resistance and drive current in the
manner described above in connection with Figures 2 and 3. DAC
440 derives control voltage CV from the current-control offset
CCNT so that the drive current of amplifier 418 equals the ODT
current Iodt calibrated in process 300. Termination elements
425 are fabricated to be identical to reference ODT resistor
230, and so respond in kind to offset signal ODT from control
system 130. In short, control system 130 calibrates a
reference termination element and a reference drive current by
establishing appropriate ODT and CCNT counts, and these counts
are applied to driver circuits 415 on the same die to
establish and maintain the correct termination resistances,
drive currents, and voltage swings.

[0038]   Receive circuit 420 does not generate a drive
current, but includes a pair of termination elements 445. Like
termination elements 425 of driver circuit 415, termination
elements 445 are calibrated by an offset ODT from the
associated ODT control system 187. Though not shown, other
embodiments include interconnected transceivers, each of which
include both drive and receive circuitry. ODT control system
187 can be used to establish appropriate termination-element
resistance, drive current, and swing voltage levels in such
embodiments. Transmission lines can be bidirectional in
systems that include interconnected transceiver pairs.

[0039]   Figure 5 details an embodiment of calibration system
200 of Figure 2, like-numbered elements being the same or
similar. In this embodiment, ODT control circuit 130 includes

additional components, many of which are included to more
closely match the behavior of the reference elements used for
calibration with the termination elements and drivers to be
calibrated. The example assumes the first reference voltage
Vr1 and input/output voltage Vio are each 1.8 volts, reference
resistance Rref is 50 ohms, swing calibration voltage Vsc is
350 millivolts, and reference current Irr is 7 milliamps;
however, these values are illustrative and not limiting.

[0040]   Terminal Vrr of comparator 215 connects to reference
resistor 175 via a pass gate 505. Pass gate 505 is included to
mirror the behavior of a pair of pass gates that are combined
to form analog multiplexer 220. Pass gate 505 offers the same
resistance as multiplexer 220, and thus cancels voltage
differences on the input terminals of comparator 215 that
would otherwise introduce errors. Complementary outputs from
comparator 215 feed an ODT counter 506 and current counter 507
via a digital filter 509 and sampling latch 510. Sampling
latch 510 periodically samples the output of filter 509. If
enabled, one of counters 506 and 507 increments or decrements
in response to the output from sample latch 510 to adjust the
count on one of buses ODT<8:0> or CCNT<6:0>. Comparator 215,
filter 509, and latch 510 are shared to save power, die area,
and to reduce offset errors in the manner discussed above in
connection with Figure 2.

[0041]   Current source 240 includes a resistor 515, a
reference current source 520, a DAC 525, and a pair of
current-source transistors 530. Resistor 515 is a replica of
ODT resistor 230, but may be of a different size or value.
Resistor 515 is formed using the same process sequence as
resistor 230, and so varies in the same manner with process,
voltage, and temperature. Current source 520 produces a
reference current Iref proportional to the value of resistor
515. DAC 525 uses reference current Iref to derive a control

voltage CCREF proportional to the resistance of resistor 515, and consequently proportional to Rodt. Current-control bus CCNT<6:0> then provides offset values to DAC 525 to adjust control voltage CCREF as necessary to calibrate currents Irr and Iodt. In one embodiment, current source 240 provides a range of output currents Irr and Iodt that range from about zero to about twice Iref. Current source 240 begins the calibration sequence in the middle of this range (Irr=Iodt=Iref).

[0042]   Current source 240 includes an additional pair of transistors 535 and 540, which serve two purposes: first, transistors 535 and 540 can disable current source 240 to save power when ODT control system 130 is not in use; second, when ODT enable signal ODTEN is asserted, transistors 535 and 540 combined with transistors 530 emulate the behavior of transistors 430 and 435 within driver 415 of Figure 4. Transistors 535 and 540 are the same size (W/L) as transistors 430, and transistors 530 combined are the same size as transistor 435. With current calibration signal ICAL2 asserted to forward bias a pair of transistors 545 and 550, transistors 530, 535, and 540 and reference ODT resistor 230 and reference resistor 175 together emulate the behavior of transistors 430 and 435 and termination elements 425 of driver circuit 415. The counts within counters 506 and 507 employed to establish appropriate termination resistances and drive currents within system 130 are therefore representative of the counts required to properly adjust the termination elements and drive currents depicted in Figure 4.

[0043]   Figure 6 depicts an ODT termination element 600 in accordance with one embodiment. Termination element 600 can be used in place of ODT resistor 230 of Figures 2 and 5 and in place of termination elements 425 and 445 of Figure 4.

[0044]   Termination element 600 includes a number of OR

gates, each of which includes one input terminal connected to a high-impedance-select terminal RHIZ. When asserted, signal RHIZ disables termination element 600, providing a high impedance between reference voltage Vio and the associated transmission line (for termination elements 425 and 445) or to multiplexer 220 (for reference ODT resistor 230). The following description assumes signal RHIZ is deasserted, so the OR gates merely pass whatever signal is provided on their respective second input terminals.

[0045]   Termination element 600 includes two separate portions: a binary-weighted portion 605 and a thermometer-coded portion 610. Portion 605 includes a resistor network 635 and a collection of PMOS transistors 630, the gates are which connected to the first six lines ODT<5:0> of control bus ODT<8:0> of Figure 5. Each PMOS transistor 630 controls the current through a respective resistive path. These resistive paths provide binary-weighted resistances from about 50 to 1600 ohms, so portion 605 can produce a wide range of resistances by enabling selected transistors 630. (The weighted resistance values can very widely with process, temperature, and voltage variations, however, hence the need for ODT calibration.)

[0046]   Transistors 630 are relatively small to reduce the effect of capacitance on transmission lines 417, so transistors 630 provide a significant percentage of the resistance through portion 605 (e.g., as much as about 30% in one embodiment). The I-V characteristics transistors 630 are somewhat non-linear, and this non-linearity produces some non-linearity in the resistance through portion 605. The first current-calibration sequence sets ODT current Iodt close to the operating current before adjusting Rodt so the non-linear response of Rodt does not introduce significant errors in Rodt when Iodt is adjusted during the swing calibration. The first

current-calibration sequence can be omitted if accuracy is
less important or if the termination elements exhibit more
linear I-V characteristics.

[0047]   The binary-weighted scheme of portion 605 provides a
relatively low capacitance, area-efficient means of producing
a large number of potential resistance values, but can
introduce problematic glitches when switching between values.
For example, incrementing the six low-order bits ODT<5:0> from
011111 to 10000 to vary the selected resistance from about 50
ohms to about 52 ohms turns off the right-most one of
transistors 630 and turns on the remaining transistors 630.
Imperfect timing can produce intermediate resistance values
significantly over or under the desired 52 ohms. Such a
resistive glitch can cause transmission errors in systems that
dynamically monitor and adjust termination values to
compensate for supply-voltage and temperature variations.

[0048]   Thermometer-coded portion 610 addresses the glitch
problem associated with portion 610. Portion 610 facilitates
fine resistance adjustments by incrementally connecting
transistors 620 in parallel with resistive elements in a
voltage divider 615. Thermometer coding means that transistors
620 are enabled one at a time, in series. The possible
combinations of signals on lines CCNT<8:6> are 000 (lowest
resistance), 100, 110, and 111 (highest resistance). Other
schemes are possible, and more or fewer series resistors can
be included. Transistors 620 are arranged in series to
minimize the effects of capacitance.

[0049]   Portion 605 is calibrated in the manner described
above and the offset provided on ODT<5:0> held steady during
operation. Portion 610 can likewise be held steady, or can be
modified continuously or periodically to compensate for
supply-voltage or temperature fluctuations. Like control bits
ODT<5:0>, control bits ODT<8:6> can be derived by a common

calibration circuit and distributed to a number of termination elements; alternatively, control bits ODT<8:6> can be derived separately for each signal pad. An ODT-control signal CNTODTb can be deasserted to disable portion 610, while calibrating portion 605, for example.

[0050]   Thermometer-coded portion 610 is less area efficient than portion 605, but can be incremented or decremented without introducing undesirable glitches. For further discussion relating to combining thermometer and binary coding, see U.S. Patent Nos. 6,606,004 and 6,297,759, each of which is incorporated herein by reference.

[0051]   Figure 7 depicts a termination element 700 in accordance with another embodiment. Termination element 700 is similar to termination element 600 of Figure 6, like numbered elements being the same or similar. Termination element 700 differs from termination element 600 in that thermometer-coded portion 610 of termination element 600 is replaced with an analog resistive element 705 to facilitate fine-tuning of termination resistance.

[0052]   The resistance between terminals Vio and Vodt includes the parallel contributions from portions 605 and 705. Portion 605 is tuned in the manner described above using an ODT count. An integrator composed of a comparator 710 and capacitor 712 then alters the gate voltage of a transistor 707 to alter the resistance through portion 705 such that voltages Vrr and Vodt are equal. The gate voltage on transistor 707 in a reference ODT termination element can be distributed to similar transistors 707 in termination elements associated with propagating signals. Alternatively, each analog portion 705 can be controlled locally using a dedicated off-chip reference resistor for each pin. In either case, portion 605 of termination elements associated with signal conveyance (e.g., elements 425 and 445) can be controlled by distributed

ODT control signals ODT<5:0>.

While the present invention has been described in connection
with specific embodiments, variations of these embodiments
will be obvious to those of ordinary skill in the art. For
example, (1) the external voltage and resistance references
may be substituted in other embodiments with on-chip
references; (2) the ODT circuits can be constructed entirely
of PMOS transistors, as PMOS transistors behave like a
resistor when operating in the linear region (e.g., with the
gate connected to ground); (3) the thermometer portion 610
(Figure 6) can have multiple "legs" connected in parallel; and
(4) one or more of the transistors 620 within thermometer
portion 610 can be replaced with a single transistor
controlled by a digital-to-analog converter. Moreover, some
components are shown directly connected to one another while
others are shown connected via intermediate components. In
each instance the method of interconnection, or "coupling,"
establishes some desired electrical communication between two
or more circuit nodes, or terminals. Such coupling may often
be accomplished using a number of circuit configurations, as
will be understood by those of skill in the art. Therefore,
the spirit and scope of the appended claims should not be
limited to the foregoing description.